AMENDMENTS

Please amend the above-identified application as follows:

In the Claims

Please cancel claims 8 and 9 without prejudice, waiver or disclaimer.

In accordance with 37 C.F.R. § 1.121, please substitute the following clean copy text for the pending claims of the same number:

(Twice amended). A circuit for detecting errors in the synchronization of a DTE (data terminal equipment) data signal with a DCE (data communication equipment) clocking signal in a communication environment wherein the DCE interfaces the DTE to a communication channel at an interface rate determined by the DCE clocking signal, the circuit comprising:

a master clock producing a master clock signal having a frequency that is an integer multiple of the frequency of the DCE clocking signal;

a clock generator deriving a circuit clocking signal from said master clock signal, said circuit clocking signal having the same frequency as the DCE clocking signal;

a sample enable generator for generating a first sample enable signal at a first time related to said circuit clocking signal and a second sample enable signal at a second time related to said master clock signal; and

a sample comparator for using said first sample enable signal, said second enable signal and said DTE data signal to determine whether the DTE data signal has undergone a transition during the time interval between said first time and said second time.

(Twice amended). A circuit for detecting errors in the synchronization of a DTE (data terminal equipment) data signal with a DCE (data communication equipment) clocking signal in a communication environment wherein the DCE interfaces the DTE to a communication channel, the circuit comprising:

means for producing a master clock signal having a frequency greater than the frequency of the DCE clocking signal;

means for deriving a circuit clocking signal from said master clock signal, said circuit clocking signal having the same frequency as the DCE clocking signal;

means for obtaining a first sample of said DTE data signal at a first time and means for obtaining a second sample of said DTE data signal at a second time, said second time being subsequent to said first time, the interval between said first time and said second time being less than the period of the DCE clocking signal;

means for comparing said first sample to said second sample;

means for generating a selector control signal if said first sample is different from said second sample;

means for inverting said circuit clocking signal to produce an inverted circuit clocking signal; and

means for selecting an output signal from the group consisting of said circuit clocking signal and said inverted circuit clocking signal, in response to said selector control signal.

10. (Twice amended). The circuit of claim 6, further comprising:

means for latching said DTE data signal.

11. (Twice amended). A method for detecting errors in the synchronization of a DTE (data terminal equipment) data signal with a DCE (data communication equipment) clocking signal in a communication environment wherein the DCE interfaces the DTE to a communication channel, the method comprising the steps of:

providing a master clock signal having a frequency that is an integer multiple of the frequency of the DCE clocking signal;

deriving a circuit clocking signal from said master clock signal, said circuit clocking signal having the same frequency as the DCE clocking signal;

obtaining a first sample of said DTE data signal at a first time based on said circuit clocking signal and a second sample of said DTE data signal at a second time based on said master clock signal, said second time being subsequent to said first time, the interval between said first time and said second time being less than the period of the DCE clocking signal; and

comparing said first sample to said second sample.

In the Drawings

Please substitute the originally filed drawings with the enclosed new formal drawings.